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NEW BURIED STRAP FORMATION METHOD FOR SUB-150 NM BEST DRAM DEVICES

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The present invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of fabricating an improved buried strap in deep trench DRAM devices in the fabrication of integrated circuits.

(2) DESCRIPTION OF THE PRIOR ART

In the fabrication of integrated circuit devices, a buried strap has been used in fabricating deep trench (DT)-based dynamic random access memory (DRAM) devices. The buried strap is a crucial part of the integration step connecting a storage node capacitor to an array switching transistor by forming a diffusion junction. Therefore, control of diffusion length and resistivity of the buried strap are key issues for a healthy interconnect between array devices and capacitors. The diffusion length and resistivity primarily depend upon buried strap width and thickness and thermal budget during post processes.

In a conventional deep trench process, a deep trench is etched. A sacrificial layer fills the trench. A first recess, recess 1, is formed by removing the sacrificial layer from an upper portion of the trench. A dielectric collar is formed conformally in the upper portion of the deep trench. The sacrificial layer is removed, buried plate doping and node dielectric are formed, and a polysilicon layer fills the trench. A second recess, recess 2, is formed to lower the top surface of the polysilicon layer below the substrate surface. A portion of the collar is removed and a second doped polysilicon layer is deposited and planarized by CMP. Now, a third recess, recess 3, is formed to lower the second polysilicon layer below the substrate surface. The buried strap is formed by dopant out-diffusion from the recessed second polysilicon layer during post recess 3 thermal processes.

However, this conventional scheme cannot accurately control the buried strap depth, thickness, and doping level because of the complex interactions of the recess 2, collar removal, and recess 3 steps. Thus, the buried strap junction diffusion is poorly controlled. The recess 3 depth is especially hard to control inasmuch as it is sensitive to both remaining silicon nitride thickness and critical dimension which are varying. A shallow etch results

in over diffusion causing short channel effects while a deep etch results in an open circuit, cutting off the current path. This limited controllability makes the BuriEd STrap (BEST) DRAM cell extendibility limited to a shorter generation.

A number of patents have addressed aspects of DRAM fabrication. U.S. Patent 6,211,006 to Tsai et al shows a trench-type capacitor. U.S. Patent 6,124,206 to Flietner et al teaches forming deep trench capacitors. U.S. Patent 6,080,618 to Bergner et al discloses formation of a buried strap with little thickness variation. The buried strap is formed where the collar is partially removed. U.S. Patent 6,008,104 to Schrems shows a BEST DRAM process. U.S. Patent 5,981,332 to Mandelman et al shows a BEST DRAM process.

SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide an effective and very manufacturable method of BEST DRAM formation in the fabrication of integrated circuits.

It is a further object of the invention to provide a method of forming an improved buried strap in DRAM device fabrication.

Another object of the invention is to provide an improved buried strap formation method using a selective hemispherical grain (HSG) method in the fabrication of a DRAM integrated circuit device.

Yet another object of the invention is to provide an improved buried strap formation method using plasma doping in the fabrication of a DRAM integrated circuit device.

A further object of the invention is to provide an improved buried strap formation method having a ground rule of less than or equal to 0.25 μm in the fabrication of a DRAM integrated circuit device.

A still further object of the invention is to provide an improved buried strap formation method using a selective HSG method along with plasma doping in the fabrication of a DRAM integrated circuit device.

In accordance with the objects of the invention, an improved buried strap method in the fabrication of a DRAM integrated circuit device is achieved. A deep trench is etched into a substrate. A collar is formed on an upper portion of the deep trench. A buried plate is formed by doping around a lower portion of the deep trench and a capacitor dielectric layer is formed within the deep trench. The deep trench is filled with a silicon layer wherein the silicon layer forms a deep trench capacitor and covers the collar. The silicon layer is recessed below a top surface of the substrate to leave a recess. A top portion of the collar is etched away to leave a collar divot. A hemispherical grain polysilicon layer is selectively deposited into the deep trench and filling the collar divot. The HSG layer is doped in-situ or by post plasma doping. The doped hemispherical grain polysilicon layer forms a buried strap in the fabrication of a deep trench DRAM integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 14 are cross-sectional representations of a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention provides an improved buried strap formation method in the fabrication of DRAM integrated circuit devices. In this invention, preferably a selective hemispherical grain (HSG) polysilicon deposition scheme is used to deposit a controlled thickness of polysilicon over an amorphous silicon layer. The process of the present invention controls buried strap thickness and doping level.

Referring now more particularly to Fig. 1, there is shown a semiconductor substrate 10. Deep trench capacitor 24 has been formed partially underlying shallow trench isolation 28. Gate electrodes and interconnection lines 30 and bit lines 36 have been formed overlying the semiconductor substrate. Buried strap 40 forms diffusion junction 42. W is the buried strap height defined by (recess 2 - recess 3) in the conventional scheme. L is the buried strap width defined by the overlap between the deep trench and the active area. The junction depth of the buried strap

diffusion junction 42 is a function of the buried strap height, temperature, and time during the post recess anneal step. Buried strap resistance is a function of the doping concentration of the second polysilicon layer, the buried strap junction depth, and buried strap width. It is desired to have a minimal buried strap resistance which defines drain sheet resistance.

Referring now to Figs. 2 through 10, the process of the invention to fabricate the BEST DRAM will be described. Referring now more particularly to Fig. 2, there is shown a portion of a semiconductor substrate 10. A silicon nitride layer 14 has been formed over the substrate. A pad oxide layer, not shown, may be formed underlying the silicon nitride layer. The silicon nitride layer has a thickness of between about 1800 and 2500 Angstroms. A a hard mask, not shown, (typically oxide such as borophosphosilicate glass with a thickness of 1200 to 1500 Angstroms) is formed over the silicon nitride layer for etching deep trenches into the substrate. In a typical process, the deep trenches are filled with a sacrificial layer which is recessed to remain only in the lower portion of the deep trenches. Then a dielectric collar layer 20 is conformally deposited in the upper portion of the deep trenches. The sacrificial layer is removed, leaving the

collar 20. The substrate around the lower portion of the trenches is doped by arsenic silicon glass (ASG) or gas phase doping (GPD), for example. A capacitor dielectric layer 52 is grown or deposited within the lower portion of the deep trenches. Then a silicon layer 54 is deposited within the deep trenches and planarized to the silicon nitride layer, as shown in Fig. 2.

Preferably, the silicon layer 54 is doped amorphous silicon. However, if the solid diffusion source is silicon germanium (Si_xGe_{1-x}), then the silicon layer 54 can be polysilicon.

Referring now to Fig. 3, the amorphous silicon layer 54 within the trenches is recessed, such as by an isotropic downstream plasma etch or by a reactive ion etch. The recess depth can be optimized to provide the optimal buried strap thickness. The recess should be between about 50 and 200 nm from the top silicon nitride surface.

Referring now to Fig. 4, the collar 20 is etched using a wet process to form a collar divot 55 of between about 30 and 50 nm below the recess 2 depth.

Referring now to Fig. 5, optionally plasma doping 57 is performed to ensure amorphous phase of the silicon layer 54. Plasma doping is an alternative implantation method for a high dose, low energy ion implantation application. A processing wafer is immersed in a plasma and is pulse biased to extract plasma ions toward the wafer. Since the plasma is a charge-neutralized media, it is not subject to space-charge limited ion extraction, thus providing a high ion flux density at a lower extraction voltage.

Referring now to Fig. 6, a silicon nitride liner or other barrier layer may be formed using chemical vapor deposition (CVD) or atomic layer deposition (ALD) methods. This liner layer 60 is formed within the collar divot 55. The liner layer may have a thickness of between about 5 and 30 nm. The liner layer is optional to the process of the invention.

Now, a buried strap is formed by a selective deposition process. A conductive layer is deposited selectively. This layer must serve as a dopant source. A selective hemispherical grain (HSG) method is preferred. If a HSG method is not used, another selective deposition method such as SiGe, selective polysilicon, or pseudo-epitaxial

silicon methods may be used. In these cases, the silicon nitride liner layer 60 is mandatory so that the conductive layer does not grow on the uncovered portion of the deep trench thereby causing a leakage path. The liner layer suppresses excess out-diffusion of dopants into the source/drain region and to prevent dislocation in the silicon layer which may cause leakage. The liner layer is optional in the HSG process because HSG will not grow on crystalline silicon due to lack of surface mobility of silicon atoms.

The preferred selective HSG polysilicon process will now be described. Preferably, the optional surface amorphization step by plasma doping has been performed to provide surface mobility of the silicon atoms in 54 to promote HSG formation. Now, selective HSG 60 is formed as is conventional in the art for stacked capacitor applications.

The polysilicon 60 (or other conductive layer) can be doped in-situ during or immediately after the deposition step. Alternatively, the polysilicon layer 60 can be doped after deposition using plasma doping, plasma ion immersion implantation (PIII), or gas phase doping (GPD) for fine dose control. Fig. 7 illustrates the alternative post-deposition doping step 65. Doping (in-situ or post-

deposition) uses arsenic or phosphorus ions for a doping concentration of between about 1E18 to 1E21 ions/cm^3.

The polysilicon layer 60 formed by HSG has a thickness of between about 20 and 100 nm and a grain size of between about 10 and 50 nm. This HSG layer will form the buried strap of the present invention. The selective HSG polysilicon deposition method deposits the buried strap polysilicon to a controlled thickness. This process avoids planarization of the buried strap layer by CMP which adds process complexity.

Optionally, a capping layer 64 may be formed over the buried strap 60, as shown in Fig. 8. The optional capping layer 64 may be used to suppress dopant loss or to minimize the surface stress which might cause dislocation into the crystalline silicon substrate. A trench top oxide or other capping layer such as silicon nitride 64 may be deposited using a selective oxidation method or by an unbiased silicon nitride liner method, whichever is appropriate for a chosen integration method, to a thickness of between about 10 and 20 nm. This additional layer may serve as a sacrificial capping layer against any contamination during or after the integration steps such as annealing or implantation steps.

Processing continues as is conventional in the art to form shallow trench isolation (STI). For example, Fig. 9 shows the formation of a hard mask 66. For example, the hard mask 66 may comprise borosilicate glass (BSG) or borophosphosilicate glass (BPSG). An antireflective coating (ARC) 68 is formed over the hard mask and a photoresist mask 70 is formed over the ARC layer.

The STI area pattern is transferred to the hard mask as shown in Fig. 10 and the photoresist mask is stripped. Now, as illustrated in Fig. 11, the deep trench area is etched into where it is not covered by the hard mask to form a STI trench 72.

Now, the hard mask is stripped using a wet etching recipe that is selective to silicon and thermal oxide as shown in Fig. 12. Now, the trench 72 is filled with an oxide layer to form a shallow trench isolation (STI) region 76. For example, the STI region is filled with an oxide using a high density plasma chemical vapor deposition (HDP-CVD) process. The oxide is planarized, for example, by chemical mechanical polishing (CMP) to complete the STI region, as illustrated in Fig. 13. The silicon nitride layer 14 serves as a polish stop during the STI CMP step.

The silicon nitride layer 14 is stripped using a wet etching process. Now, a gate oxide layer 80 is grown on the substrate surface in the active area, as shown in Fig. 14. Gate electrodes 84 are formed as is conventional in the art. Buried strap diffusion junction 86 is formed by outdiffusion from the buried strap 60 during thermal processes. The diffusion junction 86 provides a connection between the deep trench capacitor 54 and the transistor 84.

The process of the present invention provides good control of buried strap thickness and doping level. The selective deposition process used to form the buried strap, preferably a HSG process, provides simplified process steps, eliminating the recess 3 and buried strap polysilicon CMP steps. The process of the present invention is applicable to surface strap and vertical gate processes. The present invention provides low process cost and device extendibility by controlling short channel effects.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.